

## CLAIMS

What is claimed is:

- 1 1. A method comprising:  
2 receiving a packet at a network device;  
3 pre-fetching a protocol control block (PCB) associated with the packet into a  
4 cache;  
5 queuing the packet for processing; and  
6 retrieving the PCB from the cache when a processing unit is ready to process  
7 the packet.
- 1 2. The method of claim 1, further comprising pre-fetching a header associated  
2 with the packet into the cache.
- 1 3. The method of claim 2, further comprising retrieving the packet header from  
2 the cache when the processing unit is ready to process the packet.
- 1 4. The method of claim 1, further comprising sending an interrupt to notify the  
2 processing unit of the receipt of the packet.
- 1 5. The method of claim 1, wherein pre-fetching a PCB associated with the packet  
2 into a cache comprises pre-fetching a PCB associated with the packet into a cache of  
3 the processing unit.
- 1 6. The method of claim 5, further comprising storing the packet in a memory  
2 coupled to the processing unit.

- 1 7. The method of claim 1, further comprising processing the packet.
- 1 8. An apparatus comprising:  
2 a receive unit to receive a packet;  
3 a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block  
4 (PCB) associated with the packet into a cache and queue the packet for processing;  
5 and  
6 a processing unit coupled to the pre-fetch unit to retrieve the PCB from the  
7 cache and process the packet.
- 1 9. The apparatus of claim 8, wherein the receive unit is a network interface card.
- 1 10. The apparatus of claim 8, wherein the pre-fetch unit to further pre-fetch a  
2 header associated with the packet into the cache.
- 1 11. The apparatus of claim 10, wherein the processing unit to further retrieve the  
2 packet header from the cache.
- 1 12. The apparatus of claim 8, wherein the pre-fetch unit to pre-fetch a PCB  
2 associated with the packet into a cache comprises the pre-fetch unit to pre-fetch a  
3 PCB associated with the packet into a cache of the processing unit.
- 1 13. The apparatus of claim 8, further comprising an interrupt unit coupled to the  
2 receive unit and the processing unit to receive an interrupt from the receive unit and  
3 notify the processing unit of the packet.
- 1 14. An article of manufacture comprising:

2 a machine accessible medium including content that when accessed by a  
3 machine causes the machine to:  
4 receive a packet;  
5 pre-fetch a protocol control block (PCB) associated with the packet into a  
6 cache;  
7 queue the packet for processing; and  
8 retrieve the PCB from the cache when a processing unit is ready to process  
9 the packet.

1 15. The article of manufacture of claim 14, wherein the machine-accessible  
2 medium further includes content that causes the machine to pre-fetch a header  
3 associated with the packet into the cache.

1 16. The article of manufacture of claim 15, wherein the machine-accessible  
2 medium further includes content that causes the machine to retrieve the packet  
3 header from the cache when the processing unit is ready to process the packet.

1 17. The article of manufacture of claim 14, wherein the machine-accessible  
2 medium further includes content that causes the machine to process the packet.

1 18. The article of manufacture of claim 14, wherein the machine-accessible  
2 medium further includes content that causes the machine to send an interrupt to  
3 notify the processing unit of the receipt of the packet.

1 19. The article of manufacture of claim 14, wherein the machine accessible  
2 medium including content that when accessed by the machine causes the machine to  
3 pre-fetch a PCB associated with the packet into a cache comprises the machine

4 accessible medium including content that when accessed by the machine causes the  
5 machine to pre-fetch a PCB associated with the packet into a cache of the processing  
6 unit.

1 20. The article of manufacture of claim 14, wherein the machine-accessible  
2 medium further includes content that causes the machine to store the packet in a  
3 memory coupled to the processing unit.

1 21. A system comprising:  
2 a receive unit to receive a packet;  
3 a memory coupled to the receive unit to store the received packet;  
4 a memory controller coupled to the memory to manage the memory;  
5 a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block  
6 (PCB) associated with the packet into a cache and queue the packet for processing;  
7 and  
8 a processing unit to retrieve the PCB from the cache and process the packet.

1 22. The system of claim 21, wherein the receive unit is a network interface card.

1 23. The system of claim 21, wherein the pre-fetch unit to further pre-fetch a  
2 header associated with the packet into the cache.

1 24. The system of claim 23, wherein the processing unit to further retrieve the  
2 packet header from the cache.

- 1 25. The system of claim 21, further comprising an interrupt unit coupled to the
- 2 receive unit and the processing unit to receive an interrupt from the receive unit and
- 3 notify the processing unit of the packet.